EXHIBIT 15

THE HONORABLE JAMES L. ROBART

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

SRC LABS, LLC & SAINT REGIS MOHAWK TRIBE,

Plaintiffs,

v.

AMAZON WEB SERVICES, INC., AMAZON.COM, INC., & VADATA INC.,

Defendants.

CASE NO. 2:18-cv-00317-JLR

DECLARATION OF DR. HOUMAN HOMAYOUN

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

I, Houman Homayoun, Ph.D., declare as follows:

1. I have been asked by counsel for Plaintiffs to provide opinions regarding how one of ordinary skill in the art would have understood certain claim terms at issue in this lawsuit.

2. All of the opinions stated in this report are based on my personal knowledge and professional judgment. If called as a witness during the trial in this matter, I am prepared to testify competently about them. I am over the age of eighteen.

3. I am being compensated for my work in this matter but my compensation does not depend on the opinions I render or the outcome of this litigation. I do not have a personal interest in the outcome of this litigation.

II. QUALIFICATIONS

4. My *curriculum vitae* is attached as Exhibit A. A summary of my qualifications relevant to this case is provided below.

5. I am an Associate Professor of Electrical and Computer Engineering at George Mason University (GMU). I am the director of GMU's Accelerated, Secure, and Energy-Efficient Computing Laboratory (ASEEC). Prior to joining GMU, I spent two years at the University of California, San Diego, as NSF Computing Innovation (CI) Fellow awarded by the CRA-CCC working with Professor Dean Tullsen.

6. I am currently conducting research in big data computing, heterogeneous computing and hardware security and trust, which spans the areas of computer design and embedded systems, where I have published more than 80 technical papers in the prestigious conferences and journals on the subject.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

7. I am also currently leading six research projects funded by DARPA, AFRL and NSF on the topics of hardware security and trust, big data computing, heterogeneous architectures, and biomedical computing.

8. I have successfully completed four projects on "Hybrid Spin Transfer Torque-CMOS Technology to Prevent Design Reverse Engineering", "Persistence and Extraction of Digital Artifacts from Embedded Systems", "Inter-core Selective Resource Pooling in a 3D Chip Multiprocessor", and "Enhancing the Security on Embedded Automotive Systems" funded by DARPA, NIST, NSF and General Motors.

9. I received the 2016 Great Lakes Symposium on VLSI (GLSVLSI) conference best paper award for developing a manycore accelerator for wearable biomedical computing.

10. I am currently serving as Member of Advisory Committee, Cybersecurity Research and Technology Commercialization (R&TC) working group in the Commonwealth of Virginia.

11. Since 2017 I have been serving as an Associate Editor of IEEE Transactions on VLSI. He served as TPC Co-Chair for GLSVLSI 2018.

12. I am currently the general chair of GLSVLSI 2019.

III. BASIS OF OPINIONS

13. My opinions are abased on my years of education, research, experience, as well as my reading of the patents and prosecution histories. In forming my opinions I have considered the materials identified in this declaration, the patents, and the file histories.

14. I have also reviewed the declaration submitted by Brad Hutchings that is dated September 21, 2018.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

15. This declaration only represents the opinions I have formed to date. I reserve the right to revise, supplement, or amend my opinions based on new information and my continuing analysis of the patents.

IV. CLAIM CONSTRUCTION

16. I have been informed and understand that one of cannons of claim construction is that the district court must construe the claims as one of ordinary skill in the art in the relevant field of the invention would, theoretically, construe the claims, and not as a layperson would construe them. I have also been informed that the Court's claim constructions will be the basis for the jury instructions at trial so my understanding of the claim terms as one of skill in the art should be translated into plain English, to the extent that is possible, to aid the jury's understanding.

17. I have also been informed that ascertaining the meaning of the claims requires that they be viewed in the context of those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean. The Federal Circuit has stated that different weights are to be placed on these sources. First, the words of the claims themselves provide the starting point for any claim-construction analysis. The second most relevant source is the patent's specification. Third in importance is the prosecution history, which is also part of the intrinsic evidence that directly reflects how the patentee has characterized the invention. Last, extrinsic evidence—testimony, dictionaries, learned treatises, or other material not part of the public record associated with the patent—also may be helpful but is less significant than the intrinsic record in determining the legally operative meaning of claim language.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

18. I have also been informed that when determining the "ordinary meaning" a claim term the use of technical dictionaries or even a standard dictionary, such as Webster's, is often appropriate. Generally, however, technical dictionaries in the relevant field should take precedence over general dictionaries.

19. I have also been informed that § 112, ¶6 does not does not apply to a claim term if the term is understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for a structure.

20. I have been asked to provide my opinion regarding the meaning of the following claim terms using the legal principals I was instructed on above.

B. Disputed Claim Terms from the 7,149,867 Patent

1. A reconfigurable processor that instantiates an algorithm as hardware comprising:
a first memory having a first characteristic memory bandwidth and/or memory utilization; and
a data prefetch unit coupled to the memory, wherein the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory wherein the data prefetch unit operates independent of and in parallel with logic blocks using the computational data, and wherein **at least the first memory and data prefetch unit are configured to conform to needs of the algorithm**, and the data prefetch unit is configured to match format and location of data in the second memory.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

1. "a data prefetch unit coupled to the memory, wherein the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory"

Plaintiff's Proposed Construction	**Microsoft's Proposed Construction**
Not governed by 35 U.S.C. § 112, para. 6.	Governed by 35 U.S.C. § 112, para. 6. Indefinite **Function**: "retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory" **Structure**: No disclosed structure

21. My understanding is that the issue here is whether this term qualifies as means-plus-function clause subject to 35 U.S.C. § 112, ¶ 6.

22. I have been informed by counsel that to determine whether a claim term invokes means plus function treatment is a multistep inquiry. The first step is to look to see if the term uses the word "means" because if it does it does not this creates a rebuttable presumption that the term does not invoke the statutory mandates for a mean-plus-function clause.

23. Here, this term does not use the word "means" so for it to be found to be a means-plus-function clause Amazon must demonstrate that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function.

24. I have been informed that to determine whether the claim limitation describes sufficient structure to avoid being a means-plus-function limitation is evaluated based on the perspective

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

of one of skill in the art. And that a sufficient recitation of structure does not have to conjure in the mind of one of ordinary skill in the art an explicit structure for carrying out the claimed means. Rather, a general reference to a structure commonly understood by one of skill in the art to perform the function can suffice even if the lack of specific structural details results in a claim that covers a broad class of structure.

25. Counsel has informed me that the Federal Circuit has found that the following terms connote sufficient structure to avoid means-plus-function treatment:

> [T]he term "circuit," combined with a description of the function of the circuit, connoted sufficient structure to one of ordinary skill in the art to avoid 112 ¶ 6 treatment. [1]

> [T]he "system memory means" and "digital memory means" do not invoke §112, ¶ 6… A "system memory" is sufficient structure to perform the "storing data" function. To those skilled in the art, a system memory is a specific structure that stores data… In addition, the term "digital logic" designates structure to skilled artisans namely digital circuits that perform Boolean algebra. The claim also recites that the digital logic means is comprised of structural elements, including a system memory and specific modules and subsystems.[2]

26. Counsel has also informed me that the Federal Circuit has stated: "As an aid in determining whether sufficient structure is in fact recited by a term used in a claim limitation, this court has inquired into whether the "term, as the name for structure, has a reasonably well understood meaning in the art."[3]

---

[1] *Massachusetts Inst. of Tech. & Elecs. For Imaging, Inc. v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006).
[2] *TecSec, Inc. v. Int'l Bus. Machines Corp.*, 731 F.3d 1336, 1347-48 (Fed. Cir. 2013).
[3] *Watts v. XL Sys., Inc.*, 232 F.3d 877, 880–81 (Fed. Cir. 2000).

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

27. In my opinion, this claim term is not a means-plus-function clause because a "data prefetch unit" is the name for a structure that has a reasonably well understood meaning in the art.

28. Specifically, it is well understood in the art that a "data prefetch unit" is a structure (or circuit) that performs the specific functionality of prefetching the data from different levels of a memory hierarchy, which is how it is defined in the patent's specification:

> Data prefetch Unit—is a functional unit that moves data between members of a memory hierarchy. The movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory.[4]

29. The various circuits (i.e., structures) that can be used as data prefetch units have been well known in the art for decades, as shown by the figure below from a paper entitled "A Performance Study of Software and Hardware Prefetching Schemes" that was published by the IEEE in 1994:

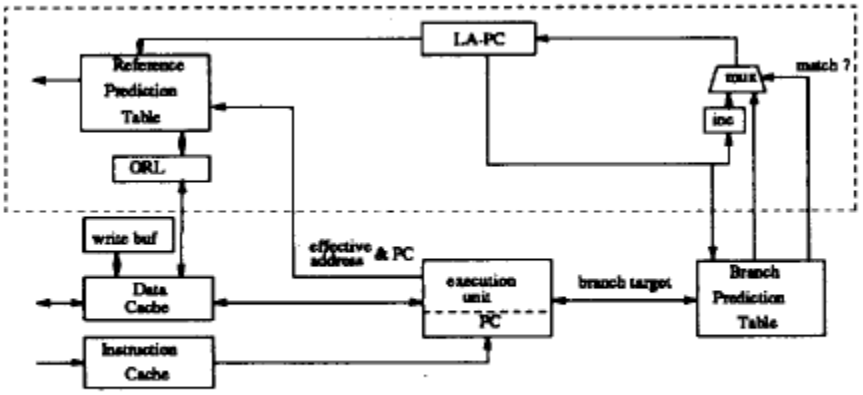


Figure 1: Structure of the hardware prefetching

[4] '867 patent, col. 5:40-43.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

30. As a result, I disagree with Dr. Hutchings' statement that: "*One of ordinary skill in the art would not understand the "data prefetch unit" term in the claim, read in light of the specification and prosecution history, to be a structural term or to carry any generally understood structural meaning in the art. Likewise, a person of ordinary skill in the art would not understand the term "unit" to connote a definite class of structures, but instead would understand that term to be a generic term akin to "means."*"

31. A data prefetch unit is the name of a type of structures, or logic circuit, that has a well understood meaning in the art.

32. In addition, the prefetch unit as indicated is a reconfigurable unit. As discussed in the description, there is no single solution fits all algorithm that can address the data prefetching needs of an arbitrary application. The specification includes several example of this.

33. Even most current state of the art processors use a number of fixed and non-programmable prefetch units which cannot be programmed and reconfigured after the fabrication. Therefore these designs cannot address the prefetching needs of future applications with different prefetching demands. These architectures were mostly designed for today's average applications.

34. A key invention disclosed in '867 is the configurability or alternatively the programmability of the prefetch unit. Invention '867 does not argue for a particular prefetch algorithm, as practically and even theoretically there is no unified one size fits all algorithm that can satisfy the demand of every possible applications (todays and future applications).

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

35. In conclusion, it is my opinion that the '867 patent does not invoke means plus function treatment regarding the "a data prefetch unit" term.

2. "at least the first memory and data prefetch unit are configured to conform to the needs of the algorithm."

Plaintiff's Proposed Construction	Microsoft's Proposed Construction
Plain and ordinary meaning and need not be construed	Indefinite

36. I've been informed that a claim term is not indefinite if when viewed in light of the specification and prosecution history it informs those skilled in the art about the scope of the invention with reasonable certainty.

37. Data prefetch units as indicated above is the name for logic circuits that move data between memories and those structures are well understood by those who have reasonable skills in the art.

38. Configuring the first memory and data prefetch unit to conform to the needs of the algorithm simply means the prefetch unit needs to be configured to conform with the size and location of the data that the processing algorithms demands. For example, if processing algorithm requires every 128 words of data and assuming that the second memory is word addressable (meaning that every word gets a unique address), then the prefetch unit needs to be configured to bring 128 words of data, discard 127 of them and only store 1 word in the first memory.

39. My understanding is confirmed by the specification, which states that the desired bandwidth efficiency gains are achieved by matching the characteristics of the data and

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

addresses provided to the prefetcher with the needs of the underlying computational logic (or "algorithm") that has been instantiated:

> The specific characteristics of the prefetch can be matched with the needs of the computational logic and the format and location of data in the memory hierarchy. For example, FIG. 9A and FIG. 9B show an external memory that is organized in a 128 byte (16 word) block structure. This organization is optimized for stride **1** access of cache based computers. A stride **128** access can result in a very inefficient use of bandwidth from the memory, since an extra 120 bytes of data is moved for every 8 bytes of requested data yielding a 6.25% bandwidth efficiency.[5]
>
> FIG. 6 shows the prefetch units 601 delivering data to the RP's onboard memory banks 305. An onboard memory bank data access unit 303 then delivers the data to computational logic 301 when required. The data prefetch units 501 couple with an intelligent memory controller 601 in the implementation of FIG. 6 that supports a strided reference pattern, which yields a 100% bandwidth efficiency in contrast to the 6.25% efficiency. Although illustrated as a single block of external memory, multiple numbers of external memories may be employed as well.[6]
>
> Again, an important feature of the present invention is the ability to implement various kinds or styles of prefetch units to meet the needs of a particular algorithm being implemented by computational elements 301. For ease of illustration, each example shows the same set of computational logic, however, in most cases the function being implemented by components 301 would change and therefore alter the decision as to which prefetch strategy is most appropriate. In accordance with the present invention, the prefetch units are implemented in a manner that is optimized for the implemented computational logic.[7]

[5] '867 patent, col. 7:49-62.
[6] '867 patent, col. 8:12-21.
[7] '867 patent, col. 9:2-13.

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

40. This is further confirmed by the prosecution history where the Examiner understood that the programmable prefetch unit contains a register which is a basic element of reconfigurablity needed to program the information regarding application memory access pattern demands.

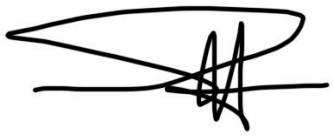
> As per claim 6, the Examiner is regarding a --register-- in its broadest reasonable sense and it thus considering it be to be a unit of logic. Therefore, the portion of the function logic that is responsible for the movement of data (as defined above to be the data prefetch unit) is being considered by the Examiner as containing a --register-- portion of the reconfigurable processor since, for instance, the blocking factor and line size of the programmable memory 112 can change, a --register-- or portion of the reconfigurable processor must be set in order to indicate the currnet line size and blocking factor when a given application is being run on the reconfigurable processor at a given point in time. Refer to paragraph 23.

41. Therefore, I disagree with Dr. Hutching's conclusion that this term does not "provide a person skilled in the art reasonable certainty of the scope of the term."

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

V. DECLARATION

42. I declare that all statements made herein are true and that these statements were made with knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: October 5, 2018

Houman Homayoun

KELLER ROHRBACK. L.L.P.
1201 THIRD AVENUE, SUITE 3200
SEATTLE, WA 98101-3053
TELEPHONE: (206) 623-1900
FACSIMILE: (206) 623-3384

EXHIBIT A

Houman Homayoun

Email: hhomayou@gmu.edu
Web: http://ece.gmu.edu/~hhomayou/
Lab: ASEEC: Accelerated, Secure, and Energy-Efficient Computing Lab
Department of Electrical and Computer Engineering
Department of Computer Science (Courtesy Appointment)
Department of Information Sciences and Technology (Courtesy Appointment)
George Mason University
Office: 3223, Engineering Building, Phone: (703) 993-5430

EDUCATION

- **Postdoc** — *Sept. 2010-Aug. 2012*

Department of Computer Science and Engineering, University of California, San Diego
Mentor: Prof. Dean Tullsen

- **PhD**

Department of Computer Science, University of California, Irvine. — *Sept. 2006-Sept. 2010*

  - Thesis: Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story.

Advisors: Prof. Alex Veidenbaum, Prof. Jean-Luc Gaudiot, Prof. Fadi Kurdahi

- **Master of Applied Science** — *September 2003-March 2005*

Electrical and Computer Engineering Department, University of Victoria, Canada.

  - Thesis: Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation.

- **Bachelor of Science** — *October 1998-May 2003*

Electrical and Computer Engineering Department, Sharif University of Technology.

EMPLOYMENT

- *Assistant Professor*, George Mason University, Department of Electrical and Computer Engineering, Courtesy Appointment with the Department of Computer Science, Courtesy Appointment with the Department of Information Sciences and Technology. — *Aug. 2012-Present*
- *Board of Advisory Member*, BroadPak Corporation, Santa Clara, California, USA. — *July 2012-Present*
- *NSF/CCC-CRA Computing Innovation Fellow*, University of California San Diego, Department of Computer Science and Engineering (Mentor: Dean M. Tullsen) — *Sept. 2010-Aug. 2012*
- *Graduate Research Assistant*, University of California, Irvine, Department of Computer Science (Advisors: Alex Veidenbaum, Jean-Luc Gaudiot and Fadi Kurdahi) — *Sept. 2006-Sept. 2010*
- *Design Architect*, Novelics Inc., Aliso Viejo, California, USA. — *Jan. 2007-Oct. 2008*
- *Researcher Assistant*, McMaster University, Canada, Department of Electrical and Computer Engineering. — *Oct. 2005-Apr. 2006*
- *Graduate Research Assistant*, University of Victoria, Canada, Department of Electrical and Computer Engineering. — *Sept. 2003-Mar. 2005*
- *Research Assistant*, Sharif University Technology, Tehran, Electronic Research Center. — *Oct. 2002-Jun. 2003*

GRANTS

Sponsored Research: Total $7,295,000, GMU Portion: $5,339,000, My Share: $4,395,000.

- *"Planning IUCRC George Mason University: Center for Hardware and Embedded System Security and Trust (CHEST)"* — *2018-2023*
  NSF IUCRC, **(PI), $15,000 for 2017-2018 planning and $750,000 (expected) over 5 years for center expenses for phase I.**
  Role: PI and Center Director on GMU site, A collaborative effort composed of George Mason University, Northeastern University, University of Connecticut, University of Texas at Dallas, University of Virginia, and Wright State University to establish the first NSF/AFRL center on HW and Embedded Systems Security and Trust.
- *"Obfuscated Logics to Enhance Security and Prevent Reverse Engineering"* — *2017-2020*

DARPA MTO Office, **(PI), $1,800,000.** ($600K fab cost to GF), **PM: Kerry Bernstein**
Role: Team lead on design and fabricating obfuscated logics in 14nm with GlobalFoundries.

- *"Mobilizing the Micro-Ops: Securing Processor Architectures via Context Sensitive Decoding"* *2018-2021*
  DARPA MTO Office, SSITH program **(PI on GMU site), Total: $1,200,000. GMU share ($400,000), PM: Linton Salmon**
  Role: Leading the team to detect HW vulnerabilities in out-of-order processors
- *"Evolution of Computer Vision for Low Power Devices, Breaking its Power Wall and Computational Complexity"* *2017-2020*
  NSF CSR-CNS, **(Co-PI)**, **$500,000**.
  Role: Developing an approximate Iterative Convolutional Neural Network coprocessor that supports approximation in memory and logic.
- *"3D-Split of Obfuscation and Authentication of logic"* *2018-2019*
  DARPA MTO Office, **(Co-PI)**, **$495,000. PM: Ken Plaks**
  Role: Developing 3D-SOUL secure-compiler for cell, route and FSM obfuscation.
- *"Persistence and Extraction of Digital Artifacts from Embedded Systems"* *2016-2017*
  NIST, National Cybersecurity Center of Excellence,
  (Co-PI), $75,000.
  Role: Establishing the persistence of digital artifacts on embedded systems through JTAG analysis.
- *"Hybrid Spin Transfer Torque-CMOS Technology to Prevent Design Reverse Engineering"* *2015- 2017*
  DARPA MTO Office, **(PI), $349,000. PM: Kerry Bernstein**
  Role: Directing the project to design and deploy new circuit methods to build reconfigurable logics to enhance performance and power efficiency.
- *"Heterogeneous Ultra Low Power Accelerator for Wearable Biomedical Computing"* *2015- 2018*
  NSF CSR-CNS, **(PI),** Total **$500,000,** GMU portion **$288,000.**
  Role: Directing the project to design and deploy new circuit methods to build reconfigurable logics to enhance performance and power efficiency.
- *"A Novel Biomechatronic Interface Based on Wearable Dynamic Imaging Sensors"* *2013- 2018*
  NSF CPS – CNS, **(Co-PI) $995,000.**
  Role: Designing a heterogeneous architecture for computing intensive biomedical application, Compare with state-of-the-art heterogeneous platforms such as TI OMAP and Nvidia Tegra.
- "*Enhancing the Security on Embedded Automotive Systems*" *2013- 2016*
  General Motors, **(Co-PI) $261,000.**
  Role: Hacking the CAN Bus Network of GM Cars.
- "*Inter-core Selective Resource Pooling in a 3D Chip Multiprocessor*" *2010- 2012*
  NSF CI Fellow Award, NSF 1019343/CRA Sub Award CIF-B-68, **(PI), $280,000**.

Equipment Support from Industry

- Nvidia Corporation: 2 Tesla K40 GPU for CNN training, **$9,560** *2017*
- Xilinx Corporation, 12 Xilinx ZYNQ board for HW accelerated computer vision, **$5,940** *2016*
- Intel Corporation, 20 Intel Galileo and Intel Edison board for wearable computing, **$2,170** *2015*

RESEARCH INTEREST

- **Big Data Computing (Current)**
  - Algorithms for energy-efficient acceleration of Big Data
  - Deep machine learning and data mining acceleration on heterogeneous platforms
  - Applied machine learning for cloud workload management, scheduling and tuning
  - Emerging big data application benchmarking and characterization on heterogeneous architectures
  - Mapping data and model parallel big data frameworks to heterogeneous accelerator architectures
- **Hardware Cybersecurity and Trust (Current)**
  - Logic obfuscation, Logic encryption, Vanishable design to prevent design reverse engineering
  - Hardware signature analysis for online malware detection
  - Detecting and containing malware epidemic in IoT network
  - Securing processor architecture against hardware vulnerability attacks

- **Heterogeneous Architecture Design and Management (Current)**
  - Design space exploration of FPGA+CPU architecture for emerging big data frameworks
  - Scheduling and resource management in heterogeneous multicore CPU+FPGA architectures
  - Accelerator design for wearable biomedical applications
  - 3D dynamic heterogeneous architecture design
- **Emerging Memory Technologies (Current)**
  - Emerging DRAM architectures in 3D (HMC, Wide I/O) for big data applications
  - Non-volatile logic and memory design
- **Power and Thermal Management**
  - Power/thermal and reliability issue in 3D architecture
  - Power management in emerging non-volatile memories
  - Power and energy optimization in VLSI circuits
  - Thermal management in emerging technologies such as 3D
  - Reliability-aware memory design
  - Dynamic power/thermal management in multi/many-core systems
  - Energy efficiency and power management in enterprise datacenter

PUBLICATIONS

(23) *"Programmable Gates Using Hybrid CMOS-STT Design to Prevent IC Reverse Engineering"* ***TODAES***
Theodore Winograd, Hassan Salmani, Hamid Mahmoodi, Kris Gaj, **Houman Homayoun**
ACM Transactions on Design Automation of Electronic Systems (Accepted)

(22) *"Low Overhead CS-based Heterogeneous Framework for Big Data Acceleration"* ***TECS***
Amey Kulkarni, Colin Shea, Tahmid Abtahi, **Houman Homayoun** and Tinoosh Mohsenin
ACM Transaction on Embedded Computing Systems, 2017 (Accepted)

(21) *"Specialized Hardware-Supported Malware Detection Using Machine Learning Techniques"* ***TDSC***
Hossein Sayadi, Nisarg Patel and **Houman Homayoun**
IEEE Transactions on Dependable and Secure Computing, 2018.

(20) *"Hardware Accelerated Mappers for Hadoop MapReduce Streaming"* ***TMSCS***
Katayoun Neshatpour, Maria Malik, **Houman Homayoun**
IEEE Transactions on Multi-Scale Computing Systems (Accepted)

(19) *"Big vs Little Core for Energy-Efficient Hadoop Computing"* ***JPDC***
Maria Malik; Katayoun Neshatpour; Setareh Rafatirad; Rajiv V Joshi; **Houman Homayoun**
Elsevier Journal of Parallel and Distributed Computing, Special Issue on Systems for Learning, Inferencing, and Discovering (SLID) (Accepted)

(18) *"Smart Grid on Chip: Work Load-Balanced On-Chip Power Delivery"* ***TVLSI***
Divya Patahk, **Houman Homayoun**, Ioannis Savidis
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, DOI: 10.1109/ TVLSI.2017.2699644, 2017

(17) "*System and Architecture Level Characterization of Big Data Applications on Big and Little Core Server Architectures*" ***TACO***
Maria Malik, Avesta Sasan, Rajiv V. Joshi, Setareh Rafatirad, **Houman Homayoun**.
ACM Transactions on Modeling and Performance Evaluation of Computing Systems (Accepted)

(16) *"Energy-Efficient Acceleration of MapReduce Applications Using FPGAs"* ***JPDC***
Katayoun Neshatpour; Maria Malik; **Houman Homayoun**
Elsevier Journal of Parallel and Distributed Computing, Special Issue on Systems for Learning, Inferencing, and Discovering (SLID) (Accepted)

(15) "*An Energy Efficient Programmable Manycore Accelerator for Personalized Biomedical Applications*" ***TVLSI***
Adam Page, Adwaya Kulkarni, Nasrin Attaran, Ali Jafari, Maria Malik, **Houman Homayoun**, and

Tinoosh Mohsenin
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Accepted)

(14) "*Heterogeneous HMC+DDRx Memory Management for Performance-Temperature Trade-offs*" ***JETC***
Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Tinoosh Mohsein, **Houman Homayoun**
ACM Journal on Emerging Technologies in Computing, 2017. (Accepted)

(13) "*Sparse Regression Driven Mixture Important Sampling for Memory Design*" ***TVLSI***
Maria Malik, Rajiv Joshi, Rouwaida Kanj, Shupeng Sun, **Houman Homayoun**, Tong Li
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Accepted)

(12) "*Hadoop Workloads Characterization for Performance and Energy Efficiency Optimizations on Microservers*" ***TMSCS***
Maria Malik, Katayoun Neshatpour, Avesta Sasan, Setareh Rafatirad, **Houman Homayoun**
IEEE Transactions on Multi-Scale Computing Systems (Accepted)

(11) "*ElasticCore: A Dynamic Heterogeneous Platform with Joint Core and Voltage/Frequency Scaling*" ***TVLSI***
Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Accepted)

(10) "*Enhancing Power, Performance, and Energy-efficiency in Chip Multiprocessors Exploiting Inverse Thermal Dependence*" ***TVLSI***
Katayoun Neshatpour, Wane Burleson, Amin Khajeh, **Houman Homayoun**
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Accepted)

(9) "*Reliability analysis of spin transfer torque based look up tables under process variations and NBTI aging*". ***MR***
Ragh Kuttappa, **Houman Homayoun**, Hassan Salmani, Hamid Mahmoodi.
Elsevier Microelectronics Reliability Journal, Volume 62, p 156-166, 2016.

(8) "*Using a Flexible Fault-Tolerant Cache to Improve Reliability for Ultra Low Voltage Operation*". ***TECS***
Abbas Banaiyanmofrad, **Houman Homayoun**, Nikil Dutt.
ACM Transactions on Embedded Computing. 14, no. 2 (2015): 32.

(7) "*Resistive Computation: A Critique*". ***CAL***
Hamid Mahmoodi, Sridevi Srinivasan Lakshmipuram, Manish Arora, Yashar Asgarieh, **Houman Homayoun**, Bill Lin and Dean M.Tullsen.
IEEE Computer Architecture Letters, DOI 10.1109/L-CA.2013.23, 2014.

(6) "*Multi-Copy Cache: A Highly Energy Efficient Cache Architecture*". ***TECS***
Arup Chakraborty, **Houman Homayoun**, Amin Khejah, Nikil Dutt, Ahmed Eltawil, Fadi Kurdahi.
ACM Transactions on Embedded Computing Systems (TECS), 2014.

(5) "*Variation Trained Drowsy Cache (VTD-Cache): A History Trained Variation Aware Drowsy Cache for Fine Grain Voltage Scaling*". ***TVLSI***
Avesta Makhzan, Kiarash Amiri, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI). VOL. 20, Issue 4, pp: 630-642. April 2012.

(4) "*MZZ-HVS: Multi Modes Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits*". ***TVLSI***
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Hsin-Cheng Yao, Shahin Golshan, Payam Heydari.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (TVLSI), VOL. 19, NO. 12, DECEMBER 2011.

(3) "*On Leakage Power Optimization in Clock Tree Networks for ASICs and General-Purpose Processors*" ***JSC***
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Alex Veidenbaum, Fadi Kurdahi.
Elsevier Journal of Sustainable Computing, Volume 1, Issue 1, March 2011, Pages 75-87 **(Invited**

paper).

(2) "*Inquisitive Defect Cache: A Means of Combating Manufacturing Induced Process Variation*". ***TVLSI***
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI), VOL. 19, NO. 9, SEPTEMBER 2011.

(1) "*Reducing Power in All Major CAM and SRAM Based Processor Units via Centralized, Dynamic Resource Size Management*". ***TVLSI***
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Jean-Luc Gaudiot.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI), VOL. 19, NO. 11, NOVEMBER 2011.

Conference Papers

2018

(82) *"Ensemble Learning for Hardware-Based Malware Detection: A Comprehensive Analysis and Classification"* ***DAC***
Hossein Syadi and **Houman Homayoun**
ACM/IEEE 55th Design Automation Conference. (DAC 2018).

(81) *"ICNN: An Iterative Implementation of Convolutional Neural Networks to Enable Energy and Computational Complexity Aware Dynamic Approximation"* ***DATE*** *Acceptance rate 24%*
Katayoun Neshatpour, Farnaz Behnia, **Houman Homayoun**, Avesta Sasan
Design, Automation & Test in Europe, (DATE 2018).

(80) "*Power Conversion Efficiency-Aware Mapping of Multithreaded Applications on Heterogeneous Architectures: A Comprehensive Parameter Tuning*" ***ASPDAC*** *Acceptance rate 31%*
Hossein Sayadi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
23rd Asia and South Pacific Design Automation Conference, (ASPDAC 2018)

(79) "Design Space Exploration for Acceleration of Machine Learning Applications". ***FCCM***
Katayoun Neshatpour, Houman Homayoun.
The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines, (FCCM 2018).

(78) "Main-Memory Requirements of Big Data Applications on Commodity Server Platform". ***CCGRID***
Hosein Mohammadi Makrani, Setareh Rafatirad and Houman Homayoun.
18th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, (CCGRID 2018).

(77) "Comprehensive Assessment of Run-Time Hardware-Supported Malware Detection Using General and Ensemble Learning". ***CF***
Hossein Sayadi, Sai Manoj, Setareh Rafatirad, Houman Homayoun.
ACM International Conference on Computing Frontiers (CF 2017).

2017

(76) *"MeNa: A Memory Navigator for Modern Hardware in Scale-out Environment"* ***IISWC*** *Acceptance rate 27%*
Hosein Makrani, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(75) *"Co-Locating and Concurrent Fine-Tuning MapReduce Applications on Microservers for Energy Efficiency"* ***IISWC*** *Acceptance rate 27%*
Maria Malik, Dean Tullsen, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(74) *"Memory Requirements of Hadoop, Spark, and MPI Based Big Data Applications on Commodity Server Class Architecture"* ***IISWC*** *Acceptance rate 27%*
Hosein Makrani, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(73) *"Analyzing Hardware Based Malware Detectors"* ***DAC*** *Acceptance*
Nisarg Patel and **Houman Homayoun**

ACM/IEEE 54th Design Automation Conference. (DAC 2017). *rate 22%*

(72) "*Big vs Little Core for Energy-Efficient Hadoop Computing*" ***DATE***
Maria Malik, Katayoun Neshatpour, Tinoosh Mohsenin, Avesta Sasan and **Houman Homayoun** *Acceptance*
Design, Automation & Test in Europe, (DATE 2017). *rate 24%*

(71) "*LESS: Big Data Sketching and Encryption on Low Power Platform*" ***DATE***
Amey Kulkarni, Colin Shea, **Houman Homayoun** and Tinoosh Mohsenin *Acceptance*
Design, Automation & Test in Europe, (DATE 2017). *rate 24%*

(70) *"Spatial and Temporal Scheduling of Clock Arrival Times for IR Hot-Spot Mitigation, Reformulation of Peak Current Reduction"* ***ISLPED***
Bhoopal Gunna, Lakshmi Bhamidipati, **Houman Homayoun** and Avesta Sasan
ACM/IEEE International Symposium on Low Power Electronics and Design, ISLPED 2017.

(69) *"A Power Delivery Network and Cell Placement Aware IR-Drop Mitigation Technique: Harvesting Unused Timing Slacks to Schedule Useful Skews"* ***ISVLSI***
Lakshmi Bhamidipati, Bhoopal Gunna, **Houman Homayoun**, Avesta Sasan
IEEE Computer Society Annual Symposium on VLSI, (ISVLSI 2017).

(68) "Machine Learning-based Approaches for Energy Efficiency Prediction and Scheduling in Composite Cores Architectures" ***ICCD***
Hossein Sayadi, Avesta Sasan, **Houman Homayoun** *Acceptance*
IEEE International Conference on Computer Design (ICCD 2017). **Runner Up for Best Paper Award.** *rate 29%*
``

(67) "Understanding the Role of Memory Subsystem on Performance and Energy-Efficiency of Hadoop Applications" (**Invited Talk**) ***IGSC***
Hosein Makrani, Shahab Tabatabaei, Setareh Rafatirad and **Houman Homayoun**
The Eighth International Green and Sustainable Computing Conference, (IGSC 2017).

(66) "Scheduling Multithreaded Applications onto Heterogeneous Composite Cores Architectures" ***IGSC***
Hossein Sayadi, **Houman Homayoun**
The Eighth International Green and Sustainable Computing Conference, (IGSC 2017).

(65) *"Work Load Scheduling For Multi Core Systems With Under-Provisioned Power Delivery"* ***GLSIVLSI***
Divya Pathak, **Houman Homayoun**, Ioannis Savidis
27th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2017).

2016

(64) "*Big Data Analytics on Heterogeneous Accelerator Architectures*" (**Invited Talk**) ***CODES-ISSS***
Katayoun Neshatpour, Avesta Sasan, **Houman Homayoun** *Acceptance*
IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis, (CODES+ISSS) 2016. *rate 23%*

(63) "*Dynamic Single and Dual Rail Spin Transfer Torque Look Up Tables with Enhanced Robustness under CMOS and MTJ Process Variations*" ***ICCD***
Aliyar Attaran, Hassan Salmani, **Houman Homayoun** and Hamid Mahmoodi
IEEE International Conference on Computer Design (ICCD), 2016.

(62) "*Hybrid STT-CMOS Designs for Reverse-Engineering Prevention*" ***DAC***
Ted Winograd, Hassan Salmani, Hamid Mahmoodi, Kris Gaj, **Houman Homayoun** *Acceptance*
ACM/IEEE 53rd Design Automation Conference. (DAC 2016). *rate 21%*

(61) "*Characterizing Hadoop Applications on Microservers for Performance and Energy Efficiency Optimizations*" ***ISPASS***
Maria Malik, Setareh Rafatirad, Rajiv Joshi, **Houman Homayoun** *Acceptance*
IEEE International Symposium on Performance Analysis of Systems and Software, (ISPASS) 2016. *rate 24%*

(60) "*Comparative Analysis of Hybrid Magnetic Tunnel Junction and CMOS Logic Circuits*". ***SOCC***
Darya Almasi, **Houman Homayoun**, Hassan Salmani, Hamid Mahmoodi
29th IEEE International System-on-Chip Conference (SOCC), 2016.

(59) "*Heterogeneous Chip Multiprocessor Architectures for Big Data Applications*". (**Invited Talk**) ***CF***
Houman Homayoun
ACM International Conference on Computing Frontiers (CF) 2016.

(58) "*Low-Power ManyCore Accelerator for Personalized Biomedical Applications*"**(Best Paper Award)** ***GLSVLSI***
Adam Page, Nasrin Attaran, Colin Shea, **Houman Homayoun,** Tinoosh Mohsenin *Acceptance rate 27%*
ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI) 2016.

(57) "*Architecture Exploration for Energy-Efficient Embedded Vision Applications: From General Purpose Processor to Domain Specific Accelerator*". ***ISVLSI***
Maria Malik, Farnoud Farahmand, Paul Otto, Nima Akhlaghi, Tinoosh Mohsenin, Siddhartha Sikdar, **Houman Homayoun**.
IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2016.

(56) "*Load Balanced On-Chip Power Delivery for Average Current Demand*" ***GLSVLSI***
Divya Pathak, Mohammad Hajkazemi, Mohammad Tavana, Houman Homayoun and Ioannis Savidis *Acceptance rate 27%*
ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI) 2016.

(55) "*Reliability Analysis of Spin Transfer Torque Based Look Up Tables Under Process Variations*" ***ISCAS***
Ragh Kuttappa, Hassan Salmani, Hamid Mahmoodi, **Houman Homayoun**
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(54) "*Energy Efficient On-Chip Power Delivery with Run-Time Voltage Regulator Clustering*" ***ISCAS***
Divya Pathak, Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi, **Houman Homayoun** and Ioannis Savidis
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(53) "*Big Biomedical Image Processing Hardware Acceleration: A Case Study for K-means and Image Filtering* ". **(Invited Special Session Talk)** ***ISCAS***
Katayoun Neshatpour, Arezou Koohi, Maria Malik, Setareh Rafatirad, Avesta Sasan, **Houman Homayoun**
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(52) "*Preventing Design Reverse Engineering with Reconfigurable Spin Transfer Torque LUT Gates*". ***ISQED***
Ted Winograd, Hasan Salmani, Hamid Mahmoodi, **Houman Homayoun**
17th International Symposium on Quality of Electronic Design, (ISQED) 2016.

2015

(51) "*System and Architecture Level Characterization of Big Data Applications on Big and Little Core Server Architectures*". ***BigData***
Maria Malik, Setareh Rafatirad, **Houman Homayoun** *Acceptance rate 17%*
IEEE BigData Conference 2015.

(50) "*Energy-Efficient Acceleration of Big Data Analytics Applications Using FPGAs*". ***BigData***
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, Avesta Sasan, **Houman Homayoun**. *Acceptance rate 17%*
IEEE BigData Conference 2015.

(49) "*Wide I/O or LPDDR? Exploration and Analysis of Performance, Power and Temperature Trade-offs of Emerging DRAM Technologies in Embedded MPSoCs*". ***ICCD***
Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana and **Houman Homayoun** *Acceptance rate 28%*
IEEE International Conference on Computer Design (ICCD), 2015.

(48) "*Big Data on Low Power Cores Are Low Power Embedded Processors a Good Fit for the Big Data Workloads?*". ***ICCD***
Maria Malik and **Houman Homayoun** *Acceptance rate 28%*
IEEE International Conference on Computer Design (ICCD), 2015.

(47) "*Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping*". ***ICCD***
Mohammad Khavari Tavana, Divya Pathak, Mohammad Hossein Hajkazemi, Maria Malik, Ioannis Savidis and **Houman Homayoun** *Acceptance rate 28%*
IEEE International Conference on Computer Design (ICCD), 2015.

(46) "*Power and Performance Characterization, Analysis and Tuning for Energy-efficient Edge Detection on Atom and ARM Based Platforms*".
Paul Otto, Maria Malik, Nima Akhlaghi, Rebel Sequeira, **Houman Homayoun** and Siddhartha Sikdar
IEEE International Conference on Computer Design (ICCD), 2015. ***ICCD*** *Acceptance rate 28%*

(45) "*Accelerating Big Data Analytics Using FPGAs*".
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, **Houman Homayoun**.
The 23rd IEEE International Symposium on Field-Programmable Custom Computing Machines, 2015. ***FCCM*** *Acceptance rate 22%*

(44) "*ElasticCore: Enabling Dynamic Heterogeneity with Joint Core and Voltage/Frequency Scaling*".
Mohammad Khavari Tavana, Mohammad Hajkazemi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
ACM/IEEE 52TH Design Automation Conference. (DAC 2015). ***DAC*** *Acceptance rate 20%*

(43) "*Just-in-time component-wise power and thermal modeling*"
Shah Mohammad Faizur Rahman, Qing Yi, **Houman Homayoun**
2015 ACM International Conference on Computing Frontiers, (CF 2015). ***CF*** *Acceptance rate 34%*

(42) "*Accelerating Machine Learning Kernels in Hadoop Using FPGAs*".
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, **Houman Homayoun**
15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, 2015. ***CCGRID*** *Acceptance rate 25%*

(41) "*Adaptive Bandwidth Management for Performance-Temperature Trade-offs in Heterogeneous HMC+DDRx Memory*".
Mohammad Hossein Hajkazemi, Michael Chorney, Reyhaneh Jabbarvand Behrouz, Mohammad Khavari Tavana and **Houman Homayoun**.
25th ACM International Conference of the Great Lakes Symposium on VLSI, 2015. ***GLSVLSI*** *Acceptance rate 28%*

(40) "*Revisiting Dynamic Thermal Management Exploiting Inverse Thermal Dependence*".
Katayoun Neshatpour, Amin Khajeh-Djahromi, Wayne Burleson, **Houman Homayoun**.
25th ACM International Conference of the Great Lakes Symposium on VLSI, 2015. ***GLSVLSI*** *Acceptance rate 28%*

2014

(39) "*Energy-efficient mapping of biomedical applications on domain-specific accelerator under process variation*".
Mohammad Khavari Tavana, Amey M. Kulkarni, Abbas Rahimi, Tinoosh Mohsenin, **Houman Homayoun**.
ACM/IEEE International Symposium on Low Power Electronics and Design, (ISLPED 2014). ***ISLPED*** *Acceptance rate 34%*

(38) "*Exploiting STT-NV Technology for Reconfigurable, High Performance, Low Power, and Low Temperature Functional Unit Design*".
Adarsh Reddy Ashammagari, Hamid Mahmoodi, **Houman Homayoun**.
Design, Automation & Test in Europe, (DATE 2014). ***DATE*** *Acceptance rate 23%*

(37) "*Enabling Dynamic Heterogeneity Through Core on Core Stacking*". **(Special Session Talk)**
Dean Tullsen, **Houman Homayoun**.
ACM/IEEE 51TH Design Automation Conference. (DAC 2014). ***DAC***

(36) "*Modeling and Analysis of Phase Change Materials for Efficient Thermal Management*".
Fulya Kaplan, Charlie De Vivero, Samuel Howes, Manish Arora, **Houman Homayoun**, Wayne Burleson, Dean Tullsen, Ayse Coskun.
International Conference on Computer Design (ICCD 2014). ***ICCD*** *Acceptance rate 25%*

(35) "*A Parallel and Reconfigurable Architecture for Efficient OMP Compressive Sensing Reconstruction*".
Amey Kulkarni, **Houman Homayoun** and Tinoosh Mohsenin.
24th ACM International Conference of the Great Lakes Symposium on VLSI, 2014. ***GLSVLSI*** *Acceptance rate 27%*

(34) "*Reconfigurable STT-NV LUT-based Functional Units to Improve Performance in General-Purpose Processors*".

Adarsh Reddy, Ashammagari, Hamid Mahmoodi, Tinoosh Mohsenin, Houman Homayoun.
24th ACM International Conference of the Great Lakes Symposium on VLSI, 2014. ***GLSVLSI***

(33) "*NVP: Non-uniform Voltage and Pulse width Settings for Power Efficient Hybrid STT-RAM*". *Acceptance rate 23%*
Reyhaneh Jabbarvand Behrouz, **Houman Homayoun**.
International Green Computing Conference, (IGCC 2014). ***IGCC***

2013

(32) "*VAWOM: Temperature and Process Variation Aware WearOut Management in 3D Multicore Architectures*"
Hossein Tajik, **Houman Homayoun**, Nikil Dutt
ACM/IEEE 50TH Design Automation Conference, (DAC 2013). ***DAC***

(31) "*Low-Current Probabilistic Writes for Power-Efficient MRAM Caches*". *Acceptance rate 23%*
Nikolaos Strikos, Vasileios Strikos, Xiangyu Dong, **Houman Homayoun**, Dean Tullsen.
International Conference on Computer Design (ICCD), 2013. ***ICCD***

(30) "*REMEDIATE: A Scalable Fault-tolerant Architecture for Low-Power NUCA Cache in Tiled CMPs*". *Acceptance rate 25%*
Abbas Banaiyanmofrad, **Houman Homayoun**, Nikil Dutt.
International Green Computing Conference. IGCC 2013. ***IGCC***

(29) *"Heterogeneous Memory Management for 3D-DRAM and External DRAM with QoS"*
Le-Nguyen Tran, **Houman Homayoun**, Fadi Kurdahi, Ahmed Eltawil.
18th Asia and South Pacific Design Automation Conference. ***ASP-DAC***

(28) *"Temperature Aware Thread Migration in 3D Architecture with Stacked DRAM"* *Acceptance rate 31%*
Dali Zhao, **Houman Homayoun**, Alex Veidenbaum.
International Symposium on Quality of Electronic Design (ISQED) 2012. ***ISQED***

(27) *" A Many-core Platform for Biomedical Signal and Image Processing"*
Jordan Bisasky, Tinoosh Mohsenin and **Houman Homayoun**.
International Symposium on Quality of Electronic Design (ISQED) 2012. ***ISQED***

2012

(26) *"Managing Distributed UPS Energy for Effective Power Capping in Data Centers"*
Vasileios Kontorinis, Baris Aksanli, **Houman Homayoun**, John Sampson, Tajana S. Rosing, and Dean M. Tullsen.
International Symposium on Computer Architecture, ISCA 2012. Portland, Oregon. ***ISCA***
Acceptance rate 17%

(25) *"Dynamically Heterogeneous Cores Through 3D Resource Pooling"*
Houman Homayoun, Vasileios Kontorinis, Ta-Wei Lin, Amirali Shayan and Dean M. Tullsen.
International Symposium on High-Performance Computer Architecture, HPCA 2012. New Orleans, Louisiana. ***HPCA***
Acceptance rate 17%

(24) *"Hot Peripheral Thermal Management to Mitigate Cache Temperature Variation"*
Houman Homayoun, Mehryar Rahmatian, Vasileios Kontorinis, Shahin Golshan, Dean Tullsen.
13th International Symposium on Quality of Electronic Design (ISQED) 2012.

(23) *"History & Variation Trained Cache (HVT-Cache):A Process Variation Aware and Fine Grain voltage Scalable Cache with Active Access History Monitoring"* ***ISQED***
Avesta Sasan, **Houman Homayoun**, Kiarash Amiri, Ahmed Eltawil and Fadi Kurdahi.
13th International Symposium on Quality of Electronic Design (ISQED) 2012. ***ISQED***

2011

(22) *"FFT-Cache: A Flexible Fault-Tolerant Cache Architecture for Ultra Low Voltage Operation"*
Abbas Banaiyan, **Houman Homayoun** and Nikil Dutt.
In Proceedings of the 2011 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, CASES 2011. Taipei, Taiwan. ***CASES***

(21) *"Reliability-Aware Placement in SRAM-based FPGA for Voltage Scaling Realization in the Presence of Process Variations"*
Shahin Golshan, Amin Khajeh, **Houman Homayoun**, Eli Bozorgzadeh, Ahmed Eltaweel and Fadi

Kurdahi.
In Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2011. Taipei, Taiwan. ***CODES-ISSS***

2010

(20) *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor*".
Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt.
5th International Conference of High Performance Embedded Architectures and Compilers, HiPEAC-2010. Italy. ***HiPEAC*** *Acceptance rate 25%*

(19) *"Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks*".
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum.
11th IEEE International Symposium on Quality Electronic Design, *ISQED-2010*. San Jose, California. ***ISQED*** *Acceptance rate 31%*

(18) *"Multiple Sleep Modes Leakage Control In Peripheral Circuits Of A All Major SRAM-Based Processor Units*".
Houman Homayoun, Avesta Sasan, Aseem Gupta, Alex Veidenbaum, Fadi Kurdahi, Nikil Dutt.
2010 ACM International Conference on Computing Frontiers, *CF-2010*. Bertinoro, Italy. ***CF*** *Acceptance rate 26%*

(17) *"Exploiting Power Budgeting in Thermal-Aware Dynamic Placement for Reconfigurable Systems"*
Shahin Golshan, Kazutoshi Wakabayashi, Benjamin Carrión Schäfer, **Houman Homayoun**, Elaheh Bozorgzadeh.
ACM/IEEE International Symposium on Low Power Electronics and Design, *ISLPED 2010*. ***ISLPED*** *Acceptance rate 24%*

(16) *"E < MC^2 : Less Energy through Multi-Copy Cache"*.
Arup Chakraborty, **Houman Homayoun**, Amin Khejah, Nikil Dutt, Ahmed Eltawil, Fadi Kurdahi.
In Proceedings of the 2010 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2010*. Scottsdale, Arizona. ***CASES***

2009

(15) *"Process Variation Aware Cache for Aggressive Voltage-Frequency Scaling*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
Design, Automation & Test in Europe, *DATE 2009*, Nice, France. ***DATE*** *Acceptance rate 23%*

(14) *"A Fault Tolerant Cache Architecture for Sub 500mV Operation: Resizable Data Composer Cache (RDC-Cache)*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
In Proceedings of the 2009 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2009*. Grenoble, France. ***CASES*** *Acceptance rate 42%*

2008

(13) *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency"*.
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.
ACM/IEEE 45TH Design Automation Conference, *DAC 2008*. Anaheim, U.S.A. ***DAC*** *Acceptance rate 23%*

(12) *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors"*.
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of the 2008 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2008*. Atlanta, U.S.A. ***CASES*** *Acceptance rate 33%*

(11) *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits"*.
Houman Homayoun, Alex Veidenbaum and Jean-Luc Gaudiot.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A. ***ICCD*** *Acceptance rate 34%*

(10) *"Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of-Order Embedded Processors"*.
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.

ACM SIGPLAN/SIGBED 2008 Conference on Languages, Compilers, and Tools for Embedded Systems, *LCTES 2008.* — ***LCTES*** *Acceptance rate 25% 17/68*

(9) *"ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits".*
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A. — ***ICCD*** *Acceptance rate 34%*

(8) *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation".*
Houman Homayoun, Mohammad Makhzan, Jean-Luc Gaudiot, and Alex Veidenbaum.
International Symposium on Systems, Systems, Architectures, Modeling and Simulation. *SAMOS VIII 2008*, Samos, Greece. — ***SAMOS*** *Acceptance rate 36%*

2007

(7) *"Reducing Leakage Power in Peripheral Circuit of L2 Caches".*
Houman Homayoun and Alexander V. Veidenbaum.
In Proceedings of IEEE International Conference on Computer Design, *ICCD 2007*. Lake Tahoe, U.S.A. — ***ICCD*** *Acceptance rate 27%*

2006

(6) "*Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation".*
Houman Homayoun and Amirali Baniasadi.
The 2nd workshop on unique chips and systems, in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software, *IEEE-ISPASS 2006*, Austin, U.S.A. — ***UCAS2-ISPASS***

(5) "*Reducing Execution Unit Leakage Power in Embedded Processors*".
Houman Homayoun and Amirali Baniasadi.
The 6th International Conference on Embedded Computer Systems, *SAMOS VI-2006*. Samos, Greece. — ***SAMOS***

(4) "*Reducing the Instruction Queue Leakage Power in Superscalar Processor*".
Houman Homayoun and Ted H. Szymanski.
The 19th Annual Canadian Conference on Electrical and Computer Engineering, *CCECE-2006*, Ottawa, Canada. — ***CCECE***

2005

(3) "*Analysis of Functional Unit Power Gating in Embedded Processors*".
Houman Homayoun and Amirali Baniasadi.
IFIP International Conference on Very Large Scale Integration System on Chip *IFIP VLSI-SOC 2005*. Perth, Wetsren Australia. — ***VLSISOC***

(2) "*Thread Scheduling Based on Low Quality Instruction Prediction for Simultaneous Multithreaded Processors*".
Houman Homayoun, Kin F. Li and Setareh Rafatirad.
The 3rd International IEEE NorthEast Workshop on Circuits and Systems, *IEEE-NEWCAS 2005*. Montreal, Canada. — ***NEWCAS***

(1) "*Functional Unit Power Gating in Simultaneous Multithreaded Processors*".
Houman Homayoun, Kin F. Li. and Setareh Rafatirad.
The IEEE Pacific Rim Conference on Communications, Computers and Signal Processing *IEEE-PACRIM 2005*. Victoria, Canada. — ***PACRIM***

PATENT

(1) Vanishable Logic To Enhance Circuit Security, U.S. Patent Application No.: 15/290,871, Filing Date: October 2016, Inventor: Houman Homayoun

HONORS/AWARDS

- **General Chair**, IEEE/ACM 29th ACM Great Lakes Symposium on VLSI. *2019*
- **Technical Program Co-Chair**, IEEE/ACM 28th ACM Great Lakes Symposium on VLSI. *2018*
- **"Associate Editor"**, IEEE Transactions on VLSI. *January 2017-January 2019*

- "**Best Paper Award**", 26th ACM Great Lakes Symposium on VLSI, GLSVLSI. *May-2016*
- "**Runner Up for Best Paper Award**", 35th IEEE International Conference on Computer Design *November-2017*
- "**National Science Foundation 2010 CI Fellowship Award**", **280,000**$ (for two years). *September-2010*
  NSF Award 1019343/CRA Sub Award CIF-B-68
  Funded Project: Inter-core Selective Resource Pooling in a 3D Chip Multiprocessor.
- **"ACM Doctoral Dissertation Nominee"**, UC-Irvine School of Information and Computer Science. *September-2010*
  (2 out of 31 PhD Dissertations were Nominated)
- **"Outstanding Graduate Student Award",** (APSIH-2010) *June-2010*
- "**4-Years Chair Fellowship Award**", University of California Irvine , **160,000**$ *September 2006-September 2010*
  Computer Science Department.
- **"DAC Student Mentor**" Award, Design Automation Conference (DAC), *June-2010*
- "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *November-2009*
  8th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.
- "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *November-2008*
  7th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.
- **"DAC Student Mentor**" Award, Design Automation Conference (DAC), *June-2008*
- "**University Scholarship***"*, McMaster University, Canada. *September 2005-August 2006*
- "**NAHAAL Scholarship***"* for Excellence in Education and Research. *September 2001-August 2002*
- "**National Ranking***"*, Rank 55 among more than 500,000 participants. *September -1998*
  Iran Nationwide Universities Entrance Exam.

STUDENTS

Alumni

PhD

1. Maria Malik, ECE Department, Fall 2013-Spring 2018, System, Architectural and Application level analysis of Big Data Applications for Performance and Energy-Efficiency
   First Job: Intel
2. Katayoun Neshatpour, ECE Department, Fall 2013-Summer 2018, Acceleration of Machine-Learning Algorithms for Big Data Applications
   First Job: Cadence

Master (with thesis)

1. Abhimanyu Chopra, Master of Science, Summer 2017
   Thesis: Optimal Allocation of Computation in IoT Network
2. Gaurav Shenoy, Master of Science, Summer 2016
   Thesis: Implementation And Evaluation Of Sat-Based Attacks On Hybrid STT-CMOS Circuits For Reverse Engineering
   Current job: Firmware Engineer at SK Hynix Memory Solutions
3. Matthew Drummond, Master of Science, Summer 2015
   Thesis: Power and Performance Characterization of Splash2 Benchmarks on Heterogeneous Architecture
   Current job: Software Engineer at Boeing
4. Adarsh Reddy Ashammagari, Master of Science, Fall 2013
   Thesis: Dynamic Functional Unit Reconfiguration using STT-RAM based Logic for Improving Performance and Mitigating Temperature Rise in Processor Architecture
   Current job: Software Engineer at Narvar

PhD Students (Current)

1. Arezou Koohi, ECE Department, Fall 2015-Summer 2018 (expected), passed PhD proposal, Machine Learning Algorithm for Biomedical Big Data Computing
2. Hosein Makrani, ECE Department, Fall 2015-Fall 2019 (expected), passed PhD RQE and TQE, Emerging Memory Technologies for Big Data

3. Hosein Sayadi, ECE Department, Fall 2015-Fall 2019 (expected), passed PhD RQE and TQE, Scheduling in Heterogeneous Architecture
4. Ted Winograd (co-advise with Kris Gaj), ECE Department, Fall 2013-Fall 2018 (expected), Hybrid CMOS+STT Technology for Hardware Security and Trust
5. Ashkan Vakil, ECE Department, Fall 2016 (co-advised with Avesta Sasan), Fall 2016-Fall 2020 (expected)
6. Farnaz Behniya, ECE Department, Spring 2017 (co-advised with Avesta Sasan), Fall 2016-Fall 2020 (expected)
7. Han Wang, ECE Department, Fall 2017-Fall 2021 (expected)
8. Mohammad Kamyar Mohajerani, ECE Department, Fall 2017-Fall 2021 (expected)
9. Ali Mirzaeian, ECE Department, (co-advised with Avesta Sasan), Fall 2017-Fall 2021 (expected), Accelerating Convolutional Neural Networks
10. Maryam Heidari (co-advise with Setareh Rafatirad), IST Department, Fall 2016-Fall 2020 (expected)
11. Gaurav Kolhe, ECE Department, Summer 2018 – Summer 2022 (expected)

Master Students with Thesis (Current)

1. Sara Bondi, Real-time Computer Vision for UAV
2. Tatiana Rodriguez, Logic Obfuscation
3. Devang Motwani, Design of wearable temperature sensor
4. Onkar Mahadev Randive, Hardware based malware detector on ARM platform
5. Sammy Lin, Modeling emerging on-chip and off-chip interconnects
6. Gaurav Kolhe, SAT-based attack modeling and simulation for reverse engineering
7. Saurabh Satish Deshpande, Accelerating convolutional neural networks

Undergraduate Student

1. Osaze Sheer (Undergraduate Research Scholars Program (URSP))
2. Nima Namazi (Undergraduate Research Scholar and Senior Design Project)
3. Tatiana Rodrigez (Undergraduate Research Scholar)
4. David Andritsis (Undergraduate Research Scholar and Senior Design Project)
5. Michael Reyes (Senior Design Project)
6. Marjorie Guillen (Senior Design Project)
7. Chris Hall (Senior Design Project)
8. Henry Pham (Senior Design Project)
9. William Johnson (Senior Design Project)
10. Graham Page (Senior Design Project)
11. Mingyu Kim (Senior Design Project)
12. Shayan Mahmoudi (Senior Design Project)
13. Jimmy Mejia (Senior Design Project)
14. Dong Pham (Senior Design Project)
15. Narek Vanetsyan (Senior Design Project)
16. Ismael Khalique (Senior Design Project)
17. Steven Wu (Senior Design Project)
18. Dai Dinh (Senior Design Project)
19. Alexander Tran (Senior Design Project)
20. Daniel Pham (Senior Design Project)

Postdoc

1. Sai Manoj Pudukotai DinakarRao, September 2017-

PhD Committee Member

1. Myeong Lim (Advisor: Jim Jones)
2. Mohamed Elsabagh (Adviosr: Angelos Stavrou)
3. Malik Umar Sharif (Advisor: Kris Gaj)
4. Rabia Shahid (Advisor: Kris Gaj)
5. Ahmad Salman (Advisor: Jens Peter Kaps)
6. Bilal Habib (Advisor: Kris Gaj)
7. Fengwei Zhang (Adviosr: Angelos Stavrou)

8. Mohammad Atiq Haque (Advisor: Hakan Aydin)
9. Nariman Mirzae (Advisor: Sam Malek)
10. Ehsan Kouroshfar (Advisor: Sam Malek)
11. Pouyan Ahmadi (Advisor: Bijan Jabbari)

Senior Design Project

1. High Frame Rate Embedded Vision for UAVs with FPGA
   M. Guillen, Ch. Hall, W. Johnson, G. Page, H. Pham, and M. Reyes
2. Compressive Sensing for Biomedical Data Acceleration on Embedded Low-Power FPGAs
   M. Kim and M. Namazi
3. Remote Motion Controller Using Leap
   D. Andritsis, D. Dinh, D. Pham, A. Tran, S. Wu
4. Remote Sensing and Processing with Low Power Bluetooth and ARM Cortex
   Sh. Mahmoudi, J. Mejia, D.H. Pham, N. Vanetsyan, and I. Khalique

Visiting Scholar

1. Professor Cheol Hong Kim, School of Electronics and Computer Engineering at Chonnam National University, South Korea, Visiting GOAL lab at GMU August 2016-August 2017.

TEACHING EXPERIENCE

Average Teaching Rating: 4.31, Average Course Rating: 4.17

- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University — *Fall 2016*
  Number of students: 23, Number of responses: 22
  Overall Teaching rating: 4.73/5, Overall for the course: 4.65/5
- **Instructor**, ECE-445 (Undergraduate-level course), Computer Organization, Department of Electrical and Computer Engineering, George Mason University — *Fall 2016*
  Number of students: 57, Number of responses: 29
  Overall Teaching rating: 3.34/5, Overall for the course: 3.36/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University — *Fall 2015*
  Number of students: 13, Number of responses: 13
  Overall Teaching rating: 4.31/5, Overall for the course: 4.38/5
- **Instructor**, ECE-699 (graduate-level course), Heterogeneous and Green Computing, Department of Electrical and Computer Engineering, George Mason University — *Spring 2015*
  Number of students: 9, Number of responses: 9
  Overall Teaching rating: 4.5/5, Overall for the course: 4.38/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University — *Spring 2015*
  Number of students: 16, Number of responses: 12
  Overall Teaching rating: 4.08/5, Overall for the course: 3.92/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University — *Fall 2014*
  Number of students: 23, Number of responses: 19
  Overall Teaching rating: 4.84/5, Overall for the course: 4.58/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University — *Spring 2014*
  Number of students: 26, Number of responses: 20
  Overall Teaching rating: 4.55/5, Overall for the course: 4.24/5

- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2013*
  Number of students: 13, Number of responses: 11
  Overall Teaching rating: 4.09/5, Overall for the course: 3.92/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University *Spring 2013*
  Number of students: 11, Number of responses: 11
  Overall Teaching rating: 4.18/5, Overall for the course: 4.00/5
- **Instructor**, ECE-641 (graduate-level course), Computer System Architecture, Department of Electrical and Computer Engineering, George Mason University *Fall 2012*
  Number of students: 15, Number of responses: 14
  Overall Teaching rating: 4.50/5, Overall for the course: 4.36/5
- **Group Leader Teaching Assistant**, leadership, management, and manufacturing engineering, University of California, Irvine, The Paul Merage School of Business *Fall 2010*
- **Teaching Assistant,** Fundamental Data Structures *Summer 2010*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant**, Logic Design Lab *Spring 2010*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant**, Senior Design Project *Fall 2009*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant,** Introduction to Computer Design *Fall 2007*
  University of California Irvine, Computer Science Department.
- **Laboratory and Tutorial Instructor**, Advanced Internet Communications *Spring 2006*
  McMaster University, Electrical and Computer Engineering Department.
- **Laboratory instructor**, General Physics *Fall 2004*
  University of Victoria, Physics Department**.**
- **Laboratory and Tutorial instructor**, Linear Circuit I *Summer 2004*
  University of Victoria, Electrical and Computer Engineering Department.
- **Laboratory instructor**, Electronic Circuit I *Spring 2004*
  University of Victoria, Electrical and Computer Engineering Department.
- **Laboratory instructor**, Microprocessor Systems *Fall 2003*
  University of Victoria, Electrical and Computer Engineering Department.
- **Tutorial instructor**, Digital Circuit Design *Summer 2002*
  Sharif University of Technology, Electrical and Computer Engineering Department.

PRESENTATIONS/INVITED TALKS/TUTORIALS

✓ *Design Space Exploration of Server Architecture for Big Data Applications*	***May 2017*** ***Masdar University***
✓ *Energy-Efficient Acceleration of Big Data Applications on Heterogeneous Architectures*	***May-2016*** ***Karlsruhe Institute of Technology***
✓ *Big Data on Heterogeneous Architectures*	***May-2016*** ***TU Dresden***
✓ *Heterogeneous Chip Multiprocessor Architectures for Big Data Applications*	***May-2016*** ***Politecnico di Milano***
✓ *Dynamic Heterogeneous Architectures in 3D*	***April-2015*** ***University of Victoria***

✓ *Heterogeneous Architectures in 3D for Next Generation Big Data Server Platform*	***Nov-2014*** ***IBM-GMU Big Data Symposium***
✓ *Big Data Applications Benchmarking and Characterization*	***Sep-2014*** ***IBM TJ Watson***
✓ *A Uniform Approach to Heterogeneity? Architectures, Tools, and Workloads for Heterogeneous Computing* ***(Special Session)***	***June-2014*** ***DAC Conference***
✓ *Dynamic Heterogeneous Architectures to Address the Efficiency Crisis* ***(Tutorial)***	***March-2014*** ***DATE***
✓ *Enabling Dynamic Heterogeneity in 3D*	***March-2014*** ***Barcelona Supercomputing Center***
✓ *Heterogeneous Architecture to Address the Efficiency Challenge!* ***(DAC Summer School)***	***June-2013*** ***DAC***
✓ *System-Level Exploration of Power, Performance, and Area for Multicore Architectures* ***(Tutorial)***	***June-2012*** ***DAC***
✓ *Future of Heterogeneous Architectures* ***(Keynote Invited Talk)***	***May-2013*** ***United States Patent Office (USPTO)***
✓ *3D Chip Multiprocessor Design*	***March-2013*** ***Virginia Tech (CESCA)***
✓ *Heterogeneous cores through 3D resource pooling* ***(Invited Interview Talk)***	***Jan-April 2012*** ***University of Wisconsin Madison, University of Central Florida, Arizona State University, University of South Florida, University of Texas San Antonio, George Mason University***
✓ *"Multiple Sleep Modes Leakage Control in Peripheral Circuits of All Major SRAM-Based Processor Units"*	***August-2011*** ***Florida International University***
✓ *"FFT-Cache:A Flexible Fault-Tolerant Cache Architecture for Low Voltage Operation"*	***November-2011*** ***9th SOC Conference***
✓ *"Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story"*	***November-2010*** ***Arizona State University***
✓ *"Power Management in High Performance Processors through Dynamic Resource Adaptation and Multiple Sleep Mode Assignments"*	***November 2010*** ***8th SOC Conference***
✓ *"Temperature-Aware SoC Optimization Framework"*	***SRC-2010*** ***Pittsburgh***
✓ *"Architectural and Circuit-Levels Design Techniques for Power and Temperature Optimizations in On-Chip SRAM Memories"*	***April-2010*** ***University of Southern California***

- ✓ *"Power, Temperature, Reliability and Performance - Aware Optimizations in On-Chip SRAM-based Caches"* ***May-2010 UCSD***
- ✓ *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor".* ***January-2010 HiPEAC***
- ✓ *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency".* ***June-2008 DAC***
- ✓ *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors".* ***October-2008 CASES***
- ✓ *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits".* ***October-2008 ICCD***
- ✓ *"Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of Order Embedded Processors".* ***June-2008 LCTES***
- ✓ *"ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On Chip SRAM Peripheral Circuits".* ***October-2008 ICCD***
- ✓ *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation".* ***July-2008 SAMOS***
- ✓ *"Reducing Leakage Power in Peripheral Circuit of L2 Caches".* ***October-2007 ICCD***
- ✓ *"Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation".* ***March-2006 UCAS2-ISPASS***

EXTERNAL SERVICE/CONFERENCE COMMITTEE MEMBER/REVIEWER

- **General Chair,** IEEE/ACM 29th Great Lake Symposium on VLSI. ***GLSVLSI-2019***
- **Technical Program Committee Co-Chair,** IEEE/ACM 28th Great Lake Symposium on VLSI. ***GLSVLSI-2018***
- **Associate Editor,** IEEE Transactions on VLSI**.** ***2017-2019***
- **National Science Foundation Panelist**. ***2013, 2014, 2015***
- **Department of Energy Panelist.** ***2013***
- **Proceeding Chair,** 27th Great Lake Symposium on VLSI. ***GLSVLSI-2017***
- **Publicity Chair**, IEEE International Conference on Big Data. ***IEEE BigData-2016***
- **Publicity Chair**, IEEE Global Communications Conference. ***GLOBECOM-2016***
- **Web Chair**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2016***
- **Web Chair**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2015***
- **TPC Co-Chair for SDM track,** IEEE International Symposium on Quality Electronic Design. ***ISQED 2015***
- **Special Session Organizer,** Harnessing the Power of Big Data – Computing Technology to Transform Big Data into Insight, the International Conference on Hardware/Software Codesign and System Synthesis. ***CODES+ISSS-2016***
- **Special Session Organizer,** A Uniform Approach to Heterogeneity**,** Design Automation Conference. ***DAC-2014***
- **Conference Session Chair,** DAC, DATE, ICCD, ISLPED, ISQED, GLSVLSI, CODES-ISSS
- **Technical Program Committee**, IEEE International Symposium on Hardware Oriented Security and Trust ***HOST-2018***
- **Technical Program Committee**, The 55st Design Automation Conference. ***DAC-2018***
- **Technical Program Committee,** IEEE International Parallel & Distributed Processing Symposium. ***IPDPS-2018***
- **Technical Program Committee,** Design, Automation & Test in Europe Conference. ***DATE-2018***
- **Technical Program Committee,** The 35th IEEE International Conference on Computer Design. ***ICCD-2017***
- **Technical Program Committee**, The 8th Green and Sustainable Computing Conference. ***IGSC-2017***
- **Technical Program Committee,** the International Conference on Hardware/Software Codesign and System Synthesis.

CODES+ISSS-2017
- **Technical Program Committee**, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems

CASES-2017
- **Technical Program Committee**, The 54st Design Automation Conference. ***DAC-2017***
- **Technical Program Committee**, Design, Automation & Test in Europe Conference. ***DATE-2017***
- **Technical Program Committee**, The 2017 ACM International Conference on Computing Frontiers. ***CF-2017***
- **Technical Program Committee**, IEEE International Symposium on Hardware Oriented Security and Trust

HOST-2017
- **Technical Program Committee**, Workshop on Attacks and Solutions in Hardware Security. ***ASHES-CCS-2017***
- **Technical Program Committee,** Euromicro Conference on Digital System Design ***DSD-2017***
- **Technical Program Committee**, The 53st Design Automation Conference. ***DAC-2016***
- **Technical Program Committee**, The 34th IEEE International Conference on Computer Design. ***ICCD-2016***
- **Technical Program Committee**, IEEE International Symposium on Performance Analysis of Systems and Software.

ISPASS-2016
- **Technical Program Committee**, 24th IEEE International Symposium on Field-Programmable Custom Computing Machines. ***FCCM-2016***
- **Technical Program Committee**, The International Conference on Hardware/Software Codesign and System Synthesis

CODES+ISSS-2016
- **Technical Program Committee**, The 26th Great Lake Symposium on VLSI. ***GLSVLSI-2016***
- **Technical Program Committee**, The 7th Green and Sustainable Computing Conference. ***IGSC-2016***
- **Technical Program Committee**, The 33nd IEEE International Conference on Computer Design. ***ICCD-2015***
- **Technical Program Committee**, The 25th Great Lake Symposium on VLSI. ***GLSVLSI-2015***
- **Technical Program Committee**, The 52st Design Automation Conference. ***DAC-2015***
- **Technical Program Committee**, The 6th Green and Sustainable Computing Conference. ***IGSC-2015***
- **Technical Program Committee**, The 32nd IEEE International Conference on Computer Design. ***ICCD-2014***
- **Technical Program Committee**, The 24th Great Lake Symposium on VLSI. ***GLSVLSI-2014***
- **Technical Program Committee**, The Fourth International Green Computing Conference. ***IGCC-2014***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2014***
- **Technical Program Committee**, The Fourth International Green Computing Conference. ***IGCC-2013***
- **Program Session Chair** of The IEEE International Symposium on Quality Electronic Design. ***ISQED-2013***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2013***
- **Technical Program Committee**, The International Symposium on Low Power Electronics Design. ***ISLPED-2012***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2012***
- **Technical Program Committee**, The 2011 ACM International Conference on Computing Frontiers. ***CF-2011***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2011***
- **Technical Program Committee**, The 9th IEEE International Conference on Computer Systems and Applications ***AICCSA-2011***
- **Reviewer,** International Symposium on High-Performance Computer Architecture. ***HPCA-2012***
- **Reviewer,** Design, Automation & Test in Europe. ***DATE-2012***
- **Reviewer**, The 19th International Conference on Parallel Architectures and Compilation Techniques. ***PACT-2010***
- **Reviewer**, The First International Green Computing Conference. ***IGCC-2010***
- **Reviewer,** The 23rd International Conference on Supercomputing. ***ICS*-2009**
- **Reviewer**, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems. ***CASES*-2009**
- **Reviewer**, The 35th International Symposium on Computer Architecture. ***ISCA-2008***
- **Reviewer**, The XXVI IEEE International Conference on Computer Design. ***ICCD-2008***
- **Reviewer**, The ACM International Conference on Computing Frontiers. ***CF-2008***
- **Reviewer**, International Symposium on Computer Architecture and High Performance Computing. ***SBAC-PAD-2007***
- **Reviewer**, International Symposium on Low Power Electronics and Design. ***ISLPED*-2009**
- **Reviewer**, the ACM Transactions on Embedded Computing Systems. ***TECS***
- **Reviewer**, The ACM Transactions on Design Automation of Electronic Systems. ***TODAES***
- **Reviewer**, The IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems. ***TCAD***
- **Reviewer**, The International Journal of Parallel Programming. ***IJPP***
- **Reviewer**, The IEEE Transactions on Very Large Scale Integration (VLSI) Systems. ***TVLSI***
- **Reviewer**, The IEEE Computer Architecture Letters ***CAL***

- **Reviewer**, IEEE Transactions on Parallel and Distributed Systems. ***TPDS***
- **Reviewer**, ACM Transactions on Architecture and Code Optimization. ***TACO***
- **Reviewer**, IEEE Transactions on Parallel and Distributed Systems. ***TPDS***
- **Reviewer,** IEEE Embedded Systems Letters. ***ESL***
- **Technical Program Committee member**, International Millennium Seminar on Electrical Engineering. ***IMSEE'2000***
- **Technical Program Committee member**, The First Educational Seminar and Specialized Course for Simulink, Electrical Engineering Department, Sharif University of Technology, *23-24 October 2000*.

INTERNAL UNIVERSITY SERVICE

- **Member of graduate recruitment committee,** Department of Electrical and Computer Engineering, GMU, 2017-present
- **Member of PhD committee,** Department of Electrical and Computer Engineering, GMU, 2016-present
- **Member of advisory to department chair committee,** Department of Electrical and Computer Engineering, GMU, 2015-2016
- **Founding Chair of distinguished talk series committee,** Department of Electrical and Computer Engineering, GMU, 2015-present
- **Member of new faculty search committee,** Department of Electrical and Computer Engineering, Computer Engineering Program, GMU, 2015
- **Member of new faculty search committee,** Department of Electrical and Computer Engineering, Computer Engineering Program GMU, 2016
- **Presentation Judge, Presenter and Advisor,** Louis Stokes Alliance for Minority Participation (LSAMP), 2015.
- **Member of PhD student proposal/dissertation committees**, Department of Electrical and Computer Engineering, Department of Computer Science, Department of Information Science and Technology, 2013-present
- **IT PhD program graduate advising**, 2015-present
- **Mentor for Office of Student Scholarship, Creative Activities, and Research (OSCAR),** Mentored undergraduate student for research in big data technology and hardware security and trust, 2016 and 2017
- **Contributed in the development of CYSE 475 Cyber Physical Systems course**, Part of new BS in Cyber Security program
- **Coordinator for computer engineering technical qualifying exam,** Department of Electrical and Computer Engineering, GMU, 2016

PROFESSIONAL EXPERIENCE

- **Graduate Researcher** *September 2006-2010*
  Center for Embedded Computer Systems, University of California Irvine,
  - Conducting research in low power, low temperature and reliability aware multi-core and memory subsystem design.
  - Developed new circuit technique referred as multi sleep mode zig-zag horizontal and vertical sleep transistor sharing to reduce leakage power in SRAM peripheral circuitry. Implemented the circuit technique in L1 and L2 Caches, Register file, Branch Predictor, Reorder Buffer and ITLB/DTLB of high performance (Core ™2 Duo) and embedded (ARM 11) processors. Developed micro-architectural approaches to control the new circuit to reduce power while maintaining performance. Developed a cycle accurate performance model based on Simplescalar and M5 micro-architecture simulator for performance and power measurements when running SPEC2K Benchmarks.
  - Developed a novel algorithm referred as access concentration and activity redistribution for reducing temperature in processor Hotspots including Register file and L1 Cache. Implemented the algorithm in MIPS-74K embedded processor register file. Used Standard Benchmarks (SPEC2K and MiBench) for evaluation.
  - Developed novel techniques for clock tree synthesis to reduce leakage power in the clock tree network. Implemented the algorithm in synopsis ASTRO back-end tool
  - Developed a new architectural approach to adapt Register File, Instruction Queue, Reorder Buffer, Load and Store Queue size in accordance with program behavior to reduce their power dissipation. Developed circuit assist to enable resource adaptation in these units.
  - Designed fault tolerant Cache architectures for process variation tolerance.

- **Design Architect** — *January 2007-October 2008*
  NOVELICS, Aliso Viejo, California
  - Principal Designer of a parametrizable BIST microcontroller for testing different memories.
  - Frond-end and back-end design including Synthesizing, floor planning, power planning and place and routing in TSMC 90nm and IBM 65nm std cell libraries using Cadence Nano-Encounter, RTL Compiler and Synopsys DC Compiler and Astro.
  - Automating the entire design and verification flow. Successful post-fabrication testing.
  - Contributing in design and verification of different embedded memories such as DRAMs and SRAMs.
- **Design/Firmware Engineer** — *May 2005-September 2005*
  Pishgam Tousee Niroo Co., Tehran, Iran
  - Designed the controller part of a commercial display monitor using Motorola 68000.
- **Graduate Researcher** — *October 2005-April 2006*
  Computer Engineering Department, McMaster University, Canada
  - Collaborated in design of a low power 5 Terabit single-chip optoelectronic VLSI crossbar switch.
- **Graduate Researcher** — *September 2003-March 2005*
  Computer Engineering Department, University of Victoria, Canada
  - Developed cycle accurate simulator to model different variety of embedded processor.
  - Developed microarchitectural techniques to increase performance and reduce power dissipation in Intel XScale processor functional units.
- **Researcher** — *October 2002-June 2003*
  Electronic Research Center, Sharif University of Technology, Tehran, Iran
  - Collaborated in designing a data acquisition system with appliance of a 16 bit Intel 196 family microcontroller as controller/supervisor and a 32 bit 6711 TI series DSP as a processor unit.
- **Service Technician** — *November 2001-April 2002*
  Internship Position, Sinatech Co.Ltd, Iran, Tehran
  - Troubleshooting medical and research laboratory appliances such as gas chromatography, atomic absorption spectrophotometry instruments, flash point tester, and cell counter instruments.
- **Software Developer** — *April 2001-July 2001*
  Internship Position, Mahab Ghods Company, Tehran, Iran
  - Design of HMI for management information system server and client application. Adding database modules and web server to management information system.